

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO. 088941/0184

Applicant: Atsushi YOSHIKAWA et al.  
Title: DELAY ADJUSTMENT CIRCUIT AND A CLOCK GENERATING  
CIRCUIT USING THE SAME  
Appl. No.: Unassigned  
Filing Date: 02/02/2001  
Examiner: Unassigned  
Art Unit: Unassigned

**PRELIMINARY AMENDMENT**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Prior to examination of the present Application, Applicants respectfully request that the above-identified application be amended as follows:

**IN THE CLAIMS:**

Claim 4, line 2, delete "any of claims 1" and insert --claim 1--;  
line 5, delete "one or more of Claims 1 through 3" and insert --claim 1--.

Claim 6, line 2, delete "any of Claim 1 through Claim 3" and insert --claim 1--;  
line 5, delete "any of Claims 1 through 3" and insert --claim 1--.

Please add the following new claims:

--12. A clock generating circuit comprising:  
the delay adjustment circuit according to claim 2 into which a reference  
clock is input; and

a logic circuit that carries out logical operations on the output signal of the delay adjustment circuit according to claim 2, and outputs a clock having an operational frequency N times said reference clock.

13. A clock generating circuit comprising:

the delay adjustment circuit according to claim 3 into which a reference clock is input; and

a logic circuit that carries out logical operations on the output signal of the delay adjustment circuit according to claim 3, and outputs a clock having an operational frequency N times said reference clock.

14. A clock generating circuit comprising:

the delay adjustment circuit described in claim 2 into which a reference clock is input;

logic circuit that carries out logical operation on a reference clock and the output signal of the delay adjustment circuit according to claim 2 and outputs a clock having an operational frequency N times that of said reference clock; and

a setting device that fixes the output of the delay adjustment circuit according to claim 2 to a constant value only during the non-operational mode; and

wherein a clock is output that has an operational frequency that is equal to that of the reference clock when serving as the non-operational mode or N times the reference clock when serving as the operational mode based on the result of the logical processing of said logic circuit.

15. A clock generating circuit comprising:

the delay adjustment circuit described in claim 3 into which a reference clock is input;

logic circuit that carries out logical operation on a reference clock and the output signal of the delay adjustment circuit according to claim 3 and outputs a clock having an operational frequency N times that of said reference clock; and

a setting device that fixes the output of the delay adjustment circuit according to claim 3 to a constant value only during the non-operational mode; and

wherein a clock is output that has an operational frequency that is equal to that of the reference clock when serving as the non-operational mode or N times the reference clock when serving as the operational mode based on the result of the logical processing of said logic circuit.

**REMARKS**

Applicants respectfully request that the foregoing amendments to Claims 4 and 6 and new Claims 12-15 be entered in order to avoid this application from incurring a surcharge for the presence of one or more multiple dependent claims.

Respectfully submitted,

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Date

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